LOW NOISE FULL INTEGRATED MULTILAYER MAGNETIC FOR POWER CONVERTERS

Related Applications

This is a continuation of United States Patent application serial number 08/351,943, filed

5   on December 8, 1994, and entitled "Low Noise Full Integrated Multilayer Magnetic for Power Converters," incorporated herein by reference.

Field of the Invention

This invention relates to DC-to-DC converters, DC-to-AC, AC-to-AC and AC-to-DC converters. The major characteristics of this power conversion technique are that all the

10   magnetic elements are implemented on the same multilayer structure, the power transfer is made highly efficient and common mode noise is minimized.

Background of the Invention

There is a continuing industry demand for increasing power density, which means more power transferred in a given volume. A method for increasing the power transfer through the

15   converter is to increase the switching frequency in order to minimize the size of magnetics and capacitors. Using prior art topologies such as forward or flyback, which employ "hard" switching techniques, makes high frequency operation less efficient. The switching losses associated with switch elements, which turn on when there is a voltage across them, are proportional with the switching frequency. An increase in switching frequency leads to an

20   increase in switching losses and an increase in level of electromagnetic interference (EMI).

In order to overcome limitations in switching speeds, the prior art has devised a new family of resonant and quasi-resonant converters. In the case of quasi-resonant converters, the prior art technique consists of shaping the current or voltage to become half-sinusoidal and to perform the switching when the current or voltage reaches zero. The reactive elements, which

25   contribute to shaping the current or voltage, are part of the basic circuit and are considered undesirable in classic topologies. An example of one such circuit can be found in Vinciarelli,

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"Forward Converter Switching at Zero Current," U.S. Patent No. 4,415,959. The technique

utilized by Vinciarelli consists of adding a resonant capacitor across the fly wheeling diode to

create a resonant circuit in combination with the leakage inductance of the transformer. During

the ON time of the main switch, a current charges the resonant capacitor. When the current

5   reaches zero, the main switch turns OFF in the primary of the transformer. The output inductor

discharges the resonant capacitor, transferring the energy to the load. This topology exhibits

several drawbacks which limit its utilization to power under 200W.

Another family of quasi-resonant converters which switch at zero voltage is described by

F. C. Lee in High Frequency Power Conversion International Proceedings (April 1987), Intertec

10   Communications, Ventura, California. These prior art circuits operate similarly to those

described above with the exception that the main switch turns ON and OFF at zero voltage.

Despite the advantage this has at the main switch, the frequency modulation which is required

for controlling the output power makes this topology unattractive.

New topologies which are referred to as "Soft Transition Technologies" were developed,

15   in order to eliminate the limitations associated with quasi-resonant and resonant converters, but

to still maintain the advantage of soft commutations for the switching elements. Such

technologies are described by I. Jitaru in "Fixed Frequency Single Ended Forward Converter

Switching at Zero Voltage," U.S. Patent No. 5,126,931, and in "Square Wave Converter Having

an Improved Zero Voltage Switching Operations," U.S. Patent No. 5,231,563. Using these

20   topologies the converter operates at constant frequency, modulating the power by varying the

duly cycle, the current and voltages on the switching elements are square-wave to decrease the

current and voltages stress, the transitions are done at zero voltage conditions, and the power is

transferred to the output, both during the ON time and OFF time.

These latest topologies have proven superior in respect of efficiency over the previous

25   resonant, and quasi-resonant topologies. However, the parasitic elements of the circuit, such as

leakage inductance and stray inductance, will negatively affect the efficiency due the circulating

energy contained in these parasitic elements. Due to the inter-winding capacitance of the

transformer the common mode noise will be injected into the secondary. In planar, low profile

magnetics required for low profile packaging the inter-winding capacitance is larger, and as a

30   result the common mode noise injected via parasitic capacitance is larger.

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Clean Version of Specification
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Brief Summary of the Invention

Power processing devices according to this invention offers a construction technique of the main transformer which also extends to all the magnetic elements, wherein the parasitic elements of the circuit are minimized. At the same time the common mode current injected to

5   the secondary via the inter-winding capacitance is reduced and even eliminated. The construction technique provided in the power processing devices of this inventions offers a simple and low cost method to further suppress the differential and common mode noise at the converter level. This novel construction technique offers an avenue to increasing the power density of the converter and allows full compliance with the requirements of safety agencies.

10   The planar multilayer magnetic is characterized by the use of flat copper spirals located on separate dielectric layers. Each layer can contain one turn or multiple spiral turns. The interconnection between the layers can be done by vias or an interconnecting trace. The insulator material can be laminated epoxy filled board, such as FR4 or a different dialectic materials. The planar multilayer structure has been described by A. Estrov in "Power

15   Transformer Design for 1Mhz Resonant Converter" at High Frequency Power Conversion in 1986. However, by decreasing the height of the planar magnetic the footprint will increase in order to maintain the same winding resistance. This will sacrifice the power density of the converter. In the exemplary embodiment of power processing devices according to this invention the transformer winding is buried between a minimum of two layers of dialectic and

20   the space on top of the winding can be populated with surface mounted components for a better volumetric efficiency. Exemplary devices in accordance with the invention provide several winding structures in a planar transformer, designed to minimize common mode noise. The exemplary embodiments further provide a full integrated multilayer structure in which all the magnetic elements are located on the same multilayer structure. The winding arrangements in

25   the input and output inductor are also structures to minimize the common mode noise. It further utilizes the inter-layer capacitance to create a low impedance for the common mode and differential mode noise, and to short it back to the source. To compensate for the common mode noise injected by the primary switching elements into the common baseplate to the secondary, the power processing devices according to the invention provide a noise cancellation technique

by injecting into the secondary a common mode current of the same amplitude, but in opposite

phase, through the common baseplate or through the multilayer structure. In certain exemplary

embodiments of the invention a packaging configuration is provided in which some of the

components of the converter are surface mounted, located on the same multilayer structure, and

5   for higher power applications, cuts in the multilayer structure allow for the body of the power

components. The heat-sink of the power components may be connected to external heat-sinks.

Brief Description of the Drawings

Figure 1 is a fragmentary cross-section view of the buried multilayer magnetic for a

10   better volumetric efficiency.

Figure 2 is a top plan view of an assembled power converter using fully integrated

multilayer magnetic.

Figure 3A is a view of an inner layer in the fully integrated multilayer magnetic which

contains a section of an input filter choke winding, a section of a transformer's primary winding

15   and a section of the output choke core.

Figure 3B is a view of an inner layer in the full integrated multilayer magnetic which

contains a section of the input choke winding, a section of the transformer's secondary winding

and a section of the output choke winding.

Figure 4 is a schematic diagram of a power conversion device that depicts the injection of

20   the common mode current through the primary to a secondary winding capacitance, due to the

voltage gradient across the primary winding of the transformer.

Figure 5 is a schematic diagram of the power conversion device like that of Fig. 4 that

illustrates the effect of a shield between primary and secondary winding in order to decrease

common mode current via the primary to secondary winding capacitance.

25   Figure 6 is a schematic diagram of a power conversion device that illustrates the use of a

differential mode and common mode input choke together with two "Y" capacitors in order to

reduce the common mode current flowing towards the input source.

Figure 7 is a schematic illustration of a typical "sandwich" layer distribution in the

transformer for a reduced leakage inductance and a reduced AC copper losses.

Figure 8 is a schematic illustration of a layer and winding distribution aimed to decreased the common mode current injection to the secondary, by locating the secondary layers between "quiet" primary layers. Quiet primary windings are those which exhibit a lower amplitude voltage swing in report to the primary ground.

5   Figure 9 is a schematic illustration of a further layer and winding distribute for common mode current reduction by using a shield between the secondary and two "quiet" primary layers.

Figure 10 is a schematic illustration of a further layer and winding distribution that provides a method for the cancellation of the common mode current into the secondary by locating the secondary layers between a "quiet" winding connected to the input DC voltage

10   source and a "noise cancellation winding" which creates a negative imagine of the common mode current injected by the first layer.

Figure 11 is a schematic illustration of a configuration in which the secondary windings are located between two symmetrical auxiliary windings, which are wound in a such way to cancel the common mode current injected to the secondary via the primary to secondary winding

15   capacitance.

Figure 12 is a schematic illustration of a configuration in which the switching element is connected in the middle of the primary winding, creating a perfect symmetry in which the common mode current injected into the secondary winding via the primary to secondary capacitance is canceled.

20   Figure 13 is a diagrammatic illustration of a winding arrangement in a magnetic element designed to reduce the inter-winding capacitance and for a better utilization of the copper.

Figure 14 is a fragmentary diagrammatic illustration of a construction using a method of compliance with IEC950 in which three layers of core material are used, for example FR4, between the primary winding and secondary winding.

25   Figure 15 is a fragmentary diagrammatic illustration of a construction using a second method of compliance with IEC950 wherein the core material between primary and secondary winding has to be thicker than .4mm.

Figure 16 is a fragmentary diagrammatic illustration of a construction using a method of compliance with safety agencies in which the magnetic core is reported to the primary and the

30   transformer does not have to be buried. The secondary winding has to comply with the creapage

distances in accordance with coating environment, based on the RMS voltages measured in the transformer.

Figure 17 is a schematic illustration of a configuration in which multiple multilayer transformers on the same multilayer structure are utilized for higher power applications or for a

5   reduced number of layers.

Detailed Description of the Preferred Embodiments

The multilayer planar magnetic, in which the windings are continuous flat copper spirals located on separate dielectric substrates, have been used before for signal and data processing. In the power conversion field the multilayer magnetic have been used since 1986. However,

10   there are several limitations with multilayer magnetic which prevented this technology from a large utilization. Decreasing the height of the magnetic, by utilizing flat windings, leads to an increased footprint. As a result a large portion of the board on which the multilayer planar magnetic is mounted, cannot be used for another purpose, having a negative impact on the volumetric efficiency. Another limitation associated with planar multilayer magnetic is the

15   increased inter-winding capacitance, which leads to higher switching losses on the switching elements and a larger common mode current injected to the secondary via the capacitance between primary and secondary windings. The parasitic elements such as the leakage inductance can be decreased in planar multilayer technology, but there is still the negative effect of parasitic elements associated with the interconnection pins. The interconnection pins will add to the cost

20   of the magnetic and also will contribute an increase in losses.

Turning now to Fig. 1 wherein a methodology of the invention is illustrated. The planar windings of the magnetic 18 are incorporated in a multilayer PCB structure 16. The top and bottom layer of the multilayer board 16 are utilized for interconnection and for pads of power components 20, or for shielding purposes or different other interconnections. By burying the

25   magnetic winding inside of the mutilayer construction the footprint of the magnetic is reduced to the footprint of the core. This allows a better utilization of the board, increasing also the power density. By burying the magnetic inside of an epoxy filled multilayer structure such as the multilayer PCB, the creapage distances requirement between the windings and the edge of the

board or cuts is decreased. This is due to the fact that the spacing between primary and secondary inside of multilayer PCB has to comply with the coating environment. These spacings are several times smaller than those in the air.

5   Another advantage of this construction technique is the fact that the interconnection between the magnetic elements, for example between the transformer and output choke are done through the same multilayer PCB, eliminating the need for interconnection pins. The power components can be located on top of the multilayer PCB, interconnecting with the magnetic winding through vias, or can be located on an external heatsink, using cuts in the PCB tailored to the body of power components as is depicted in Fig. 2. In Fig. 2 is presented a fully integrated

10   multilayer PCB power converter structure which incorporates all the magnetic elements such as the input filter 10, the main transformer 12, and the output choke 14. The body of the power components is accommodated by using cuts in the multilayer PCB structure. The connection of power components to the windings is done by through holes in which the terminals of the components can be soldered. For lower power levels the power components are located on top

15   of the PCB and through vias or large parallel pads of low thermal impedance extended to the bottom of the multilayer PCB to which an external heatsink can be attached. The additional heatsink may not be required if there is an air flow on top of the converter.

The magnetic core 18 has legs penetrating through the multilayer PCB. The core will create a closed magnetic path with or without an air gap, as a function of the electrical topology

20   in which it is utilized.

In Fig. 3A the structure of an inner layer contains a section of the input choke winding 22 and a section of the primary winding 24 of the transformer. The cores of the input choke 10, main transformer 12 and output choke 14, penetrate through the multilayer PCB. The vias 26, are designed to interconnect the windings from different layers. Some of the vias are designed to

25   interconnect the magnetic windings to the components located on the top and bottom of the multilayer PCB.

In Fig. 3B the structure of an inner layer is shown which contains another section of the input choke winding 22, a section of the secondary winding 28 of the transformer and a section of the winding 30 of the output choke. The connection from the transformer to output choke is

done directly without supplementary interconnections. This will minimize the stray inductance associated with the interconnection pins.

One of the novel aspects of this invention is the integration of all the magnetic elements on the same multilayer structure. For better utilization of space, the magnetic windings are buried

5   inside, allowing the top and bottom layer to be utilized for locating surface mounted components. This leads to a very efficient utilization of the volume due to a three dimensional utilization. This form of integration leads to a minimization of the interconnection impedance and as result leads to a higher efficiency in power processing. The available area on the board of Figs. 3A and 3B is the area on the top and bottom surfaces not taken up by the footprints of the cores 10, 12

10   and 14 and thus available for mounting circuit components. Mounting components directly above or below the footprints of the windings 22, 24, 28 and 30 and their end connection pads in the embodiment of Figs. 3A and 3B frees up slightly more than 30% of the available area for this purpose. Using this real estate on the top and/or bottom surfaces of the multilayer PCB thus enables greatly improving the converter's power density. In a converter like that depicted in

15   Figs. 3A and 3B in excess of 25% of the surface of the board (the total area inside the perimeter of the board) is made unavailable by the magnetic cores 10, 12 and 14. If the winding footprints are excluded from the area to be populated by surface mounted circuit components then the real estate on surfaces of the board that can be used to mount these components is reduced by nearly half.

20   The multilayer PCB magnetic offers a good avenue in addressing the creapages and clearance requirements demanded by the safety agencies. By burying the transformer inside of the PCB as is depicted in Fig. 14, the spacing between primary and secondary is determined in accordance with the RMS voltages in transformer applied to a coating environment. These spacing are several times smaller than those in the air. However, between primary and

25   secondary windings two or three layers of core material 92, 94, 96 are demanded, each two able to withstand the dielectric test. Another method requires the core material between the primary and secondary 98, to be at least .4mm. The magnetic core can be reported to the primary or to the secondary. In Fig. 16 an exemplary embodiment is shown in which the core is reported to the primary. The secondary windings 104 are buried inside and the distance from the secondary

30   winding 104 to the edge of the core slow has to comply with the creapage requirements for the

RMS voltage measured in the transformer. Using this method the primary winding 102 and the interconnecting vias do not have to be buried in the multilayer PCB.

The AC voltage gradient across each turn of the winding is equal, but reported to the input ground the amplitude of the voltage swing increases from the turn connected to the input

5   DC source to the maximum level to the turn connected to the switching element. As is depicted in Fig. 4, the voltage swing 32 across the primary winding injects a current in the secondary winding 38 via the primary to secondary winding capacitance 34, 36. This current is further flowing through the decoupling capacitor 40, through the earth ground 44, returning through the connections of the input and output leads of the power supply and is a noise parameter that is

10   measured by the FCC and VDE.

As depicted in Fig. 5, one method of suppressing some of the common mode (CM) noise is utilizing a shield 54, or two located between primary and secondary winding and connected to the input DC source or the input ground. The capacitance between the shield 54 and the primary winding creates a low impedance path for the common mode current created by the AC voltage

15   across the primary winding 32. However the stray impedance of the shield itself will create a voltage gradient across it which will inject a common mode current via the capacitance 56 between the shield and the secondary winding 38. This common mode current 42, is reduced in comparison to the structure without the shield. However, the parasitic inductance of the connection to the input DC source 46, is critical for shielding effectiveness. One of the major

20   drawback associated with the use of the shield is the fact that an increased parasitic capacitance will be created across the primary winding and across the secondary winding. This will increase the switching losses on the switching elements. This parasitic capacitance 52 will be in parallel with the inter-winding capacitance of the primary and the parasitic capacitance of the switch itself. The switching losses will become more significant at higher operation frequency and for

25   high input voltage applications such as off-line converters.

In Fig. 7, in a winding arrangement in a converter, the secondary windings 80 are sandwiched between the primary windings. For simplicity, I consider that the primary winding of the transformer is contained in four layers and the secondary winding is one layer. The winding of layer 1 connected to the input voltage source 72, exhibits a lower voltage swing

30   reported to the input ground comparative to the winding 78 of layer 4 connected to the switching

element 70. In this particular case the voltage swing reported to the primary ground is four times larger for layer 4, 78 than for the layer 1, 72. It is logical to locate the secondary 80 in the vicinity of the "quiet" primary such as 72. However the secondary has to be located symmetrically between primary windings for two reasons. One reason is to minimize the

5   magnetic field intensity between windings for lower AC copper loss, and the second reason is to lower the leakage inductance between primary and secondary.

In order to decrease the common mode current injection into the secondary via the capacitance between primary winding to secondary winding, and maintaining at the same time the sandwiched structure, the configuration of Fig. 8 is suggested. In Fig. 8 the secondary

10   winding is located between two quiet layers. The voltage swing across layer 1 is much smaller than the voltage swing across layer 3. This structure does not eliminate the common mode injection to the secondary but it will reduce it. The advantage of this configuration is the fact that it does not require any addition layer.

In Fig. 9 is a configuration in which two layers on the top and the bottom of the

15   secondary are used as a shield 54. The location of the shield in vicinity of two "quiet" layers, layer 1, 72 and 2, 74, will not increase significantly the parasitic capacitance across the primary winding. However two layers of the multilayer structure will be allocated to the shield 54.

A configuration which can reduce the common mode noise injection to the secondary to zero is depicted in Fig. 10. In this configuration a noise cancellation winding 82, is added. The

20   polarity of the voltage swing across this winding is opposite to the polarity of the voltage swing across the winding in a layer 1. As a result the common mode current injected into the secondary winding will be canceled. This method will require only one additional layer and if a perfect geometrical symmetry can be accomplished, the common mode current injected in the secondary can be totally canceled. The single drawback of this is the fact that one layer will be

25   allocated just for the noise cancellation.

In Fig. 11 two layers are added, one on top and one on the bottom of the secondary winding. These windings have a common symmetrical connection which is connected to the input ground. The connection can be also to the input DC voltage source. The voltage swing across the winding 1, 84 and auxiliary winding 2, 86 will inject a common mode current into the

30   secondary, but of the opposite polarity of each other. As a result the total common mode current

injected to the secondary will be zero. These auxiliary windings can be utilized to provide power in the primary section such as the necessary bias power, or can provide the power for the primary reported output.

5   Another path for the common mode current is through the capacitance between the switching elements in the primary and in the secondary, and the baseplate. This applies for higher power applications in which a common heatsink baseplate is used for the power components in the primary and secondary circuits. Due to a large voltage swing of the power switch tab, this source of common mode noise can be dominant. This invention claims a method for cancellation of the common mode current produced by the switching elements. This is done

10   by creating a supplementary capacitor between the secondary and the termination of the noise cancellation winding not connected to the input DC source or input ground. The noise cancellation windings are shown in Fig. 10 and Fig. 11. By properly tailoring this additional capacitance a current will be injected into the secondary, of the same amplitude but in opposite phase to the current injected by the switching elements to the secondary via the capacitance

15   between the switches and the baseplate. The additional capacitance between the noise cancellation winding and secondary can be implemented in the metal baseplate or in the multilayer structure.

      Another method which does not require supplementary layers for output common mode noise cancellation is presented in Fig. 12. In this case the primary winding is symmetrically cut

20   in half and the power switch is connecting to these sections. The voltage swing on the layers which surrounds the secondary, layer 2, 74 and layer 3, 76, will have the same amplitude but will be of opposite polarity. As a result the common mode noise injected into the secondary will be zero.

      The structures presented above will reduce the common mode noise injection to the

25   secondary via the inter-winding capacitance of the transformer. However, if the common mode noise will be generated by different circuitry or if a further reduction of common mode is required, a supplementary common mode filter may be required. Such a structure is shown in Fig. 6. By utilizing a EE or EI core gapped in the center leg, the input choke can exhibit a common mode and a differential mode impedance. By using the outer legs of the core, two

30   inductive elements can be implemented in the PCB. The coupling between these inductor will

determine the CM impedance, and it can be tailored by the gapping configuration of the core. For example, if there is not a gap in the core, the coupling coefficient is K=.071. If there is 1 mill gap in all the legs, K=.276. If only the center leg is gapped to 2 mil, K=.724. The common mode and differential mode inductance can be tailored by properly gapping the core, and making

5   sure that under all loading conditions the core does not saturate. Utilizing full integrated multilayer PCB, the cost of the input EMI filter is reduced to the cost of the magnetic core. The capacitors 62, and 64 are used to create a low impedance for the common mode current which will work against the high impedance exhibited by the input filter. The capacitors 62 and 64 can be created in the structure of the multilayer PCB, which will lead to a cost reduction of the

10   converter and to a better utilization of the multilayer structure. These capacitors can be constructed to comply with the safety agencies by using the recommendations suggested for the transformer compliance with safety agencies, previously discussed.

Fig. 13 provides reduction of the parasitic capacitance across the magnetic winding. This is accomplished by shifting the adjacent layers. For a better utilization of the copper, the turn

15   width is varied in such a way to ensure an equal resistance per each turn. The turn width is made larger as one moves from the inside turn to the outermost turn so that the winding resistance for the shorter turn can be equal to the winding resistance for the longer turn. For higher power applications or in applications which require large currents multiple planar multilayer transformers can be utilized on the same multilayer structure as is depicted in Fig. 17. The

20   number of layers in primary 112, 114, 116 and in the secondary 118, 120, 122 of these transformers 106, 120, 122 can be reduced to one, which will allow the use of two layer multilayer structure. Another advantage of this configuration is the fact that the leakage inductance in each transformer can be very low, which will make this configuration ideal for high current and low output voltage.

25   Many alternations and modifications may be made by those having ordinary skill in the art without departing from the spirit and scope of the invention. Therefore, the invention must be understood as being set forth above only for the purpose of example and not by way of limitation. The invention is defined by the following claims wherein means may be substituted therein for obtaining substantially the same result even when not obtained by performing

30   substantially the same function in substantially the same way.